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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/625,812	07/26/2000	Timothy J. Van Hook	0007057-0012/000105 B S	8263

23600 7590 02/12/2003

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EXAMINER
SINGH, DALIP K

ART UNIT	PAPER NUMBER
2676	

DATE MAILED: 02/12/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/625,812	VAN HOOK, TIMOTHY J.	
	Examiner	Art Unit	
	Dalip K Singh	2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 4-7, 9-10, 19-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6, 493,820 B2 to Akkary et al. in view of U.S. Patent No. 6,223,276 B1 to Lee et al.

a. Regarding claim 1, Akkary et al. **discloses** a programmable graphics processor (processor 50, Figure 2) for executing a plurality of programs (...thread management logic 124 creates different threads from a program or process...col. 5, lines 24-67; col. 6, lines 1-4), said programmable graphics processor (processor 50) comprising: an execution pipeline (execution pipeline 108) having a pipeline latency (...there may be...various...latency, etc...col. 26, lines 35-40); an interleaver (thread management logic 124) for interleaving instructions (...a thread includes the trace...a trace is a...instruction...col. 5, lines 20-25) from said plurality of programs (...threads are either from completely independent programs or are from the same program...col. 1, lines 63-65) and providing said instructions (...a thread includes the trace...a trace is a...instruction...col. 5, lines 20-25) to said pipeline (execution pipeline 108) for execution. Akkary et al. **does not address** the issue of each one of said programs having an apparent latency

less than said pipeline latency (...there may be...various...latency, etc...col. 26, lines 35-40). Lee et al. **discloses** the significance of latency problem and addresses this issue in its invention (col. 1, lines 28-44). Therefore, it would have been obvious to one of ordinary skill in the art at the time invention was made to modify the device as taught by Akkary et al. with the feature "programs having an apparent latency less than the said pipeline latency" as taught by Lee et al. because it provides a way to avoid performance bottleneck in a fixed pipeline depth (col. 1, lines 28-44).

b. Regarding claim 4, Akkary et al. **discloses** wherein each program of said plurality of programs is independent of the other of said plurality of programs (...threads...these processors process and execute are independent of each other...col. 1, lines 58-64).

c. Regarding claim 5, Akkary et al. **discloses** including an output buffer (ROB 164 and MOB 178) for storing out of order data output (...the result of an execution and related information...written to...re-order buffer (ROB) 164...col. 7, lines 36-50).

d. Regarding claims 6 and 7, Akkary et al. **discloses** including one or more of a register copy (thread management logic 124), program counter (program counters 112A,...112X...col. 5, lines 25-30), and program counter stack (thread management logic 124) provided for each of said plurality of programs, and further **discloses** wherein one or more of control and computing resources, instructions, instruction memory, data paths, data memory, and caches are shared by said plurality of programs (Figure 1 and 2).

e. Regarding claims 9 and 10, Akkary et al. **discloses** wherein said instructions comprise load instructions for loading data from a data memory (load buffers 182, Figure 3), and store instructions for storing data in a memory (store buffers 184, Figure 3) and wherein said data memory (MOB 178) comprises a cache (data cache 176).

f. Regarding claim 19, it is similar in scope to claim 5 above and is rejected under the same rationale.

a. Regarding claim 20, Akkary et al. **suggests** the use of no-op (bubbles in the pipeline...col. 13, lines 35-42).

g. Regarding claim 21, Akkary et al. **suggests** loading new programs when one of said register slots is available (col. 7, lines 30-35).

3. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6, 493,820 B2 to Akkary et al. in view of U.S. Patent No. 6,223,276 B1 to Lee et al. as applied to claim 1 above, and further in view of U.S. Patent No. 5,961,628 to Nguyen et al.

a. Regarding claim 8, Akkary et al. and Lee et al. **implicitly disclose** SIMD execution of vector instructions without addressing vector lengths. Nguyen et al. **explicitly discloses** wherein said processor executes SIMD vector instructions of vector length N and executes in parallel a plurality of instructions having SIMD vector lengths that sum up to N (col. 1, lines 11-24; col. 53-60). Therefore, it would have been obvious to one of ordinary skill in the art at the time invention was made to modify the device as taught by Akkary-Lee combination with the feature "SIMD vector instructions execution of vector length L and plurality of

instructions having SIMD vector lengths summing up to N" as taught by Nguyen et al. **because** it provides a way to reduce processing time for repetitive task (col. 1, lines 10-25).

4. Claims 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6, 493,820 B2 to Akkary et al. in view of U.S. Patent No. 6,223,276 B1 to Lee et al. as applied to claim 1 above, and further in view of U.S. Patent No. 5,973,705 to Narayanaswami.

a. Regarding claims 12 and 13, Lee et al. **does not disclose** a graphics processor wherein address space of said data memory comprises a frame buffer unit and a texture memory unit as it describes a vector processor in general with possible suggestion of its use in multimedia processing (col. 1, lines 10-25). Narayanaswami **discloses explicitly** a SIMD graphics processing system comprising a frame buffer unit (frame buffer 110f, Fig. 2A) while **implicitly** suggesting a texture memory unit. Therefore, it would have been obvious to one of ordinary skill in the art at the time invention was made to modify the device as taught by Akkary-Lee combination with the feature "frame buffer and texture memory unit" as taught by Narayanaswami **because** it provides a way to reduce processing time (col. 2, lines 20-22).

5. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6, 493,820 B2 to Akkary et al. in view of U.S. Patent No. 6,223,276 B1 to Lee et al. as applied to claim 1 above, and further in view of U.S. Patent No. 5,778,250 to Dye.

a. Regarding claim 2, Akkary-Lee et al. combined teachings **does not address** the limitation wherein said pipeline (execution pipeline 108) has a

datapath with a depth equal to said number of programs. Dye **discloses** the pipeline stages being dynamically adjusted for simpler or complex operations resulting in increased speed and performance of the processor (col. 3, lines 1-11). Therefore, it would have been obvious to one of ordinary skill in the art at the time invention was made to modify the device as taught by Akkary-Dye combination with the feature "dynamically adjustable pipeline stages of an execution pipeline" as taught by Dye **because** it provides a way to improve the overall speed and performance of the processor (col. 3, lines 1-11; col. 5, lines 5-10).

6. Claims 3 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6, 493,820 B2 to Akkary et al. in view of U.S. Patent No. 6,223,276 B1 to Lee et al. as applied to claim 1 above, and further in view of U.S. Patent No. 6,209,083 B1 to Naini et al.

b. Regarding claim 3, Lee et al. **does not disclose** wherein a next instruction from one of said plurality of programs (...threads are either from completely independent programs or are from the same program...col. 1, lines 63-65) is not provided to said pipeline (execution pipeline 108) until a previous instruction of said one of said plurality of programs (...threads are either from completely independent programs or are from the same program...col. 1, lines 63-65) has completed. Naini et al. **discloses** working in the same respect as the claim limitation "...processor will not issue a next...instruction...until the previously issued...instruction has cleared...col. 2, lines 1-5". Naini et al. further indicates that the previous instruction will not have an exception (col. 2, lines 1-

5). The application specification is clear in detailing avoiding the hardware complexity of pipeline bypasses, instruction reordering or the inefficiencies of idle cycles (page 11, 1st paragraph) in much the same fashion. Therefore, it would have been obvious to one of ordinary skill in the art at the time invention was made to modify the device as taught by Akkary- Lee combination with the feature "no next instruction into the pipeline until the previous instruction has completed or retired from the pipeline" as taught by Naini et al. **because** it provides a way to reduce pipeline stalling, or the need for pipeline bypass, instruction reordering or idle cycles in the pipeline (col. 1, lines 59-60).

c. Regarding claim 14, it is similar in scope to claim 3 above and is rejected under the same rationale.

d. Regarding claims 15 and 16, they are similar in scope to claim 6 above and are rejected under the same rationale.

e. Regarding claim 17, it is similar in scope to claim 2 above and is rejected under the same rationale.

f. Regarding claim 18, it is similar in scope to claim 8 above and is rejected under the same rationale.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following prior art teach SIMD processing and execution of pipelines in superscalar processors.

U.S. Patent No. 6,470,445 B1 to Arnold et al.

U.S. Patent No. 6,064,818 to Brown et al.

U.S. Patent No. 5,420,990 to McKeen et al.

U.S. Patent No. 5,428,807 to McKeen et al.

U.S. Patent No. 5,710,912 to Schlansker et al. U.S. Patent No. 6,282,635 to Sachs

U.S. Patent No. 5,802,386 to Kahle et al. U.S. Patent No. 5,949,996 to Atsushi

U.S. Patent No. 6,161,173 to Krishna et al. U.S. Patent No. 6,209,078 to Chiang et al.

U.S. Patent No. 5,548,737 to Edrington et al. U.S. Patent No. 5,809,552 to Kuroiwa et al.

U.S. Patent No. 6,412,061 to Dye

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Dalip K. Singh** whose telephone number is **(703) 305-3895**. The examiner can normally be reached on Mon-Thu (8:00AM-6: 30PM) Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Matthew Bella**, can be reached at **(703) 308-6829**.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 305-0377.

dks

February 8, 2003

MATTHEW C. BELLA
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600